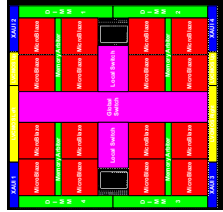


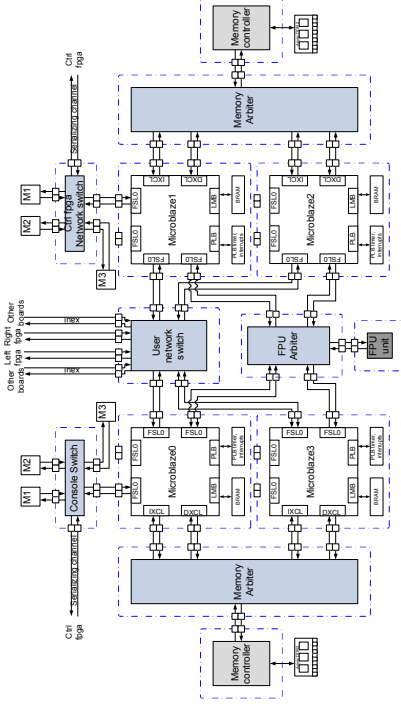
RAMP Blue Architecture, Implementation and RDL

Introducing RAMP Blue

- **First RAMP System**
Debugging & Design of RAMP Infrastructure Pushed the Xilinx FPGAs tools Drove BEE2, BEE3 & RDL Development
- **Technical Details**
Originally implemented in Xilinx EDK Uses Xilinx MicroBlaze for processor Nodes 8-12 MicroBlazes per FPGA 1-21 Boards (Tested so far) All-To-All embedded in Ring embedded in 3D Mesh
- **Currently a System not an Emulator**
An artifact of the design process RDL was not done when RAMP Blue started Upcoming RDL release is the first step



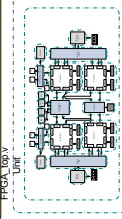
Architecture & RDL Implementation



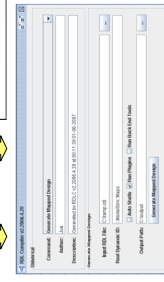
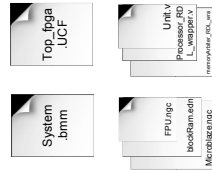
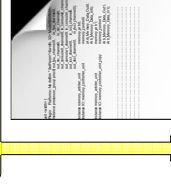
- **Communication modules** (e.g. XAUI, serializer) replaced by RDL channels
- **Standard port interface** - different units can be swapped in place of each other easily
- **Time dilation through unit** and channel parameters, for performance research

Design & Tool Flow

top_fpga.v responsible for BEE2 board level infrastructure, and non-unit Verilog modules.

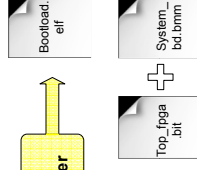


System level netlist written in RDL. Includes parameterization & replication.

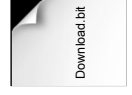


RDL C2 Auto-Generated ISE Project. Includes BlackBoxes from EDK, all RDL unit implementations, and constraints. Will switch to XFlow eventually...

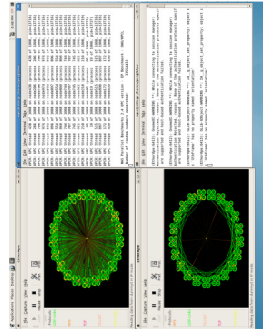
Compile bootloader



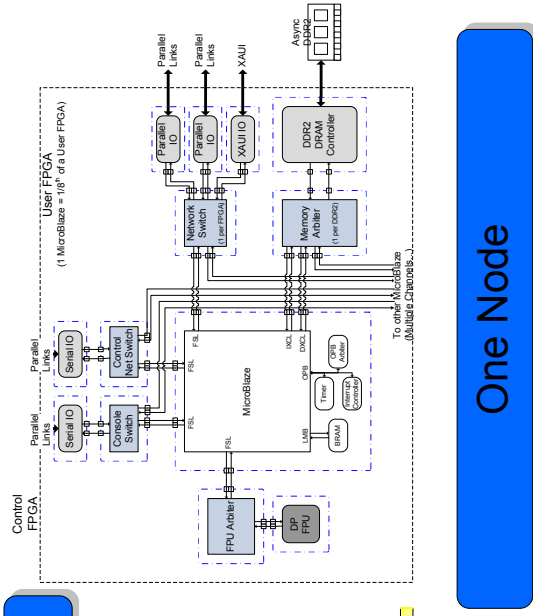
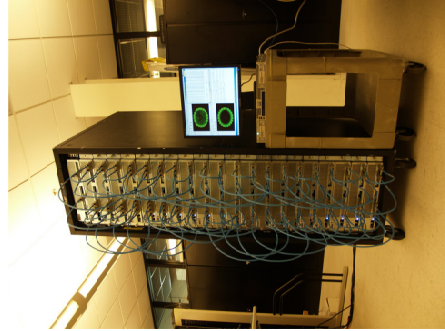
Generate a bitfile in ISE



Run data2mem generate a bit file that initialize bram for each MB with bootload code



In Action



One Node